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(54) Title of the Invention: **A Probe for Testing Semiconductor Integrated Circuits and a Test Method Using Said Probe**

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1. **[Title of the Invention] A Probe for Testing Semiconductor Integrated Circuits and a Test Method Using Said Probe.**

2. **[Limits of the Patent Claims]**

[Claim 1] A semiconductor integrated circuit test probe which is characterized by provision of a semiconductor substrate, by formation of multiple needle-shaped protuberances upon one surface of said semiconductor substrate surface by selective etching, by electrical isolation of the respective needle-shaped protuberances from each other by an isolation method, and by connection of said needle-shaped protuberances to an external circuit by a beam lead structure.

[Claim 2] A semiconductor integrated circuit test probe per Claim 1 characterized by selective etching of the surface of said semiconductor substrate to form multiple protuberances, said protuberances having a flat surface.

[Claim 3] A method for manufacture of a semiconductor device, said method being characterized by inclusion of a step which performs characteristic testing while contacting said needle-shaped protuberances of the previously mentioned test probe of Claim 1 and Claim 2 to the pads formed upon the wafer or chip

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containing the semiconductor integrated circuit being tested.

3. **[Detailed Explanation of the Invention]**

[Summary] This invention pertains to a test probe for use in the testing of wafer or chip semiconductor integrated circuits. One surface of a semiconductor substrate is selectively etched to form multiple needle-shaped protuberances upon said semiconductor substrate (the respective protuberances being electrically isolated from each other by an isolation process) and a means for contacting said needle-shaped protuberances to an external circuit via a beam lead structure, with the goal of making highly reliable contact with the pads arrayed upon a high density integrated circuit, said pads being on the order of 10 μm across.

[Field of Industrial Application] This invention pertains to a test probe for use during the testing of wafer or chip semiconductor integrated circuits.

[Prior Art] The processes for manufacture of a semiconductor integrated circuit may be roughly divided into the procedures that form semiconductor circuits within regions of the chip or wafer, the processes that divide the resultant wafer into separate chips, and processes that end in the completion of the individual chip packages. Static and dynamic characteristic testing is performed upon the wafer integrated circuits that were formed during these processes. Integrated circuits are selected for subsequent processing after these characteristic tests. A test probe containing multiple metallic probe needles is made to temporarily electrically connect the above mentioned integrated circuit to an external test circuit (signal generator, power source, etc.) to perform these characteristic tests.

Figure 6 shows the structure of the prior art probe used for the above mentioned tests. As shown in Figure 6 (a), multiple probe needles 3, made from tungsten, are fixed to the top surface of a printed circuit board provided with a central aperture roughly 30 mm in diameter. Palladium and beryllium/copper are also used for these probe needles 3. As shown in Figure 6 (b), the tip of each probe needle 3 is bent so as to protrude toward the bottom surface of the printed circuit board through aperture 2. The position of the far end of respective probe needles 3 corresponds to the location of pads provided upon the integrated circuit chip. Such pads, for example, may be spaced 200 μm apart in a square pattern. The opposite end of probe needle 3 is contiguous with interconnects 4 upon printed circuit board 1 which connect to board contacts 5.

During testing one integrated circuit region upon the wafer is aligned within the central hole 2. Then the tips of probe needles 3 are pushed into contact with the various pads provided at the periphery of the integrated circuit chip. Test signals and electrical power voltage are supplied via board contacts 5.

[Problems that the Invention is to Solve] The above mentioned prior art test

probe has two major problems:

(1) When the tips of probe needles 3 are pushed against the integrated circuit chip 11 pads, as shown in Figure 7, rubbing against the pads 11 occurs in the lateral direction. Item 3, drawn with dashed lines, shows the probe needle 3 prior to the occurrence of lateral movement. This movement may easily result in damage to pad 11, which is constructed from aluminum, etc. Such pad damage may result in problems during the subsequent bonding process. In particular bonding may become impossible when the ball-bonding method is used for the connections between integrated circuit chip 10 and the external circuitry.

(2) Since the tips of the multiple tungsten, etc. probe needles extend several centimeters from their fixed ends, it is difficult to assure precise placement upon the tested integrated circuit chip pads, which are spaced roughly 200 μm apart. Moreover, it is difficult to say if the mechanical strength of the probe needles is sufficient since the tip of probe needle 3 must mechanically collide with and may get caught upon the tested circuit, resulting in probe needle tip deformation.

Also as the density of semiconductor integrated circuits is increased, the number of connections with the external circuitry increase. Therefore the surface area upon the integrated circuit covered by pads increases. Therefore it becomes necessary that the pad surface area and spacing should be reduced so that the fraction of the surface occupied by pads does not increase.

It is relatively easy to reduce the surface area and spacing of the pads upon the integrated circuit. Although dimensional control is possible on the order of a micron, placing the prior art test probe needles 3, as shown in Figure 6, with sufficient degree of dimensional precision is a problem. It has been difficult to accomplish such testing using the prior art test probe.

This invention provides a test probe which can solve the above mentioned problems of the prior art. Moreover the goal of this invention is to make possible testing of large scale integrated circuits using such a test probe.

[Means for Solution to the Problems] This invention achieves the above goals by providing a semiconductor integrated circuit test probe which is characterized by provision of a semiconductor substrate, by formation of multiple needle-shaped protuberances upon one surface of said semiconductor substrate surface by selective etching, by electrical isolation of the respective needle-shaped protuberances from each other by an isolation method, and by connection of said needle-shaped protuberances to an external circuit by a beam lead structure.

Also this invention is a semiconductor integrated circuit test probe as per Claim 1 characterized by selective etching of the surface of said semiconductor

substrate to form multiple protuberances, such protuberances having a flat surface. Also this invention is a method for manufacture of a semiconductor device, said method being characterized by inclusion of a step which performs characteristic testing while contacting said needle-shaped protuberances of the previously mentioned test probe to pads upon the wafer chip containing the semiconductor integrated circuit being tested.

[Operation of the Invention] The contacts used for the test probe of this invention are formed by the small scale fabrication techniques established for semiconductor integrated circuit manufacture. An array consisting of multiple minute closely spaced needle-shaped protuberances are formed simultaneously.

Specifically:

(1) Needle-shaped protuberances are formed upon a semiconductor substrate by anisotropic etching of the semiconductor crystal.

(2) The respective contacts are formed isolated electrically from each other by use of the techniques such as those used during semiconductor integrated circuit manufacture for isolation of circuit elements.

(3) One type of semiconductor integrated circuit bonding technology that may be used to connect the respective contacts to an external circuit is the beam lead method.

Therefore it becomes possible to effectively conduct characteristic testing of large scale integrated circuits using this test probe, as was previously done with the prior technology for less dense circuits. The probe of this invention may be used to examine large scale integrated circuits upon a wafer, even when the tested integrated circuit chip pad spacing and size are so small as to require high precision placement of test probe contacts. Furthermore since the tips of all of the test probe contacts are within the same plane, it is no longer necessary to use additional pressure against the pads of the tested integrated circuit to assure uniform contact. Also damage, as was seen with the prior art test probe to the tested integrated circuit pads, is lessened since lateral movement does not occur.

[Embodiments of the Invention] Below the invention is explained while referring to illustrations.

Figure 1 shows a partial diagram of the test probe of this invention for testing semiconductor integrated circuits. Silicon chip 10 has the same size as the tested semiconductor integrated circuit. Upon one surface of silicon chip 10 are formed multiple contacts by an etching process. The tips of respective probe contacts 11 have a needle shape and are placed so as to correspond one-to-one to the positions of pads upon the tested integrated circuit. The respective probe

contacts 11 are electrically isolated from each other by means that will be explained later.

Upon silicon chip 10 are provided means for connection to an external circuit. For example, such means might be a structure such as beam lead electrodes 12, a well-known method. Within the center of silicon chip 10 is provided a visual observation window 14. This visual observation window 14 is used to perform alignment of the tested integrated circuit chip and the test probe of this invention.

Probe contacts 11 are formed into a cone shape by an etching process. These cones bite into the aluminum metal pads as the test probe is pushed against the pads of the integrated circuit chip during testing. Therefore damage is possible when contact pressure is increased such that the contact breaks through the pad metal layer to the insulation and dopant-containing layers of the semiconductor substrate beneath. To avoid this problem and to simplify the test procedure, it is advantageous to use probe contacts constructed as shown in Figure 2 (a).

In other words, needle-shaped protuberances 22 are formed above multiple planar protuberances 21 by selective etching of silicon chip 10. As shown in Figure 2 (b). The planar surface of contact 20 of Figure 2 (a) butts up against the pad 25 formed upon the tested integrated circuit chip 24 when the test probe is pressed against the tested integrated circuit chip 24. By this means deep scoring of pad 25 by probe contact 22 is prevented.

The method of manufacture of the test probe of this invention is explained while referring to Figure 3.

One side of a silicon wafer is oxidized. After the SiO_2 layer is formed, the SiO_2 layer is etched using well-known lithography techniques. SiO_2 mask layer 31 spots 20 μm in diameter are formed upon the previously mentioned silicon wafer 30 surface. Figure 3 (b) shows the cross section indicated by X-X within Figure 3 (a). The spacing of the SiO_2 mask layer 31 spots is the same as the pads upon the (unillustrated) integrated circuit chip under testing. For example, these SiO_2 mask layer 31 spots may be spaced 40 μm apart.

Next the silicon wafer 30 is etched around the SiO_2 mask layer 31 to a depth 10 μm using, for example, a well-known mixed isotropic etchant solution containing nitric and hydrofluoric acids. During this etching process silicon wafer 30 is etched in the vertical direction as well as beneath the SiO_2 layer mask spots in the lateral direction due to the side etching effect. Since the mass of silicon removed by this side etching increases as the distance from the original silicon wafer surface decreases, as the surface is etched to a depth of 10 μm, needle-shaped protuberances 32 are left behind beneath the SiO_2 mask layer 31 spots, as shown in Figure 3 (c). The height of the needle-shaped protuberances

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32 is roughly 10 μm.

A <100> crystal orientation silicon wafer 30 is used. The etching rate depends upon crystal orientation. For example, an etchant solution such as KOH may be used to form needle-shaped protuberances 32 by isotropic etching. It is also possible to form non-cone-shaped needle-shaped protuberances 32. Also it is possible to deposit beforehand a doped silicon layer 10 μm thick upon the silicon wafer 30 so as to easily control the etched mass and hence shape of the needle-shaped protuberances 32. Such a dopant-containing surface layer could be formed upon the silicon wafer 30 surface by epitaxial growth.

It is possible to form the probe contacts 20 shown in Figure 2 by first forming needle-shaped protuberances 22 and then placing resist layer over protuberances 21, which include the needle-shaped protuberances 22. The uncovered silicon wafer surface then undergoes anisotropic etching.

After the remnant SiO_2 mask layer 31 is removed, a SiO_2 layer is formed upon the silicon wafer 30 surface by thermal oxidation. The surface is coated with resist. Then this resist layer is exposed and developed. As shown in Figure 3 (d), an opening is formed in the resist coating, This opening in the resist 35 includes needle-shaped protuberances 32 as well as the neighboring contact regions 34. Figure 3 (e) shows a cross-sectional view of the Y-Y transect indicated in Figure 3 (d). Item 36 is the previously mentioned SiO_2 layer. The pattern of resist mask 35 covers the 10 μm step region which includes needle-shaped protuberance 32. It is also possible to use an exposure method other than positive resist / e-beam exposure.

Next the remnant resist is removed to leave SiO_2 layer 36 as a mask. Dopant is diffused into the remaining clear silicon wafer surface 30 of the needle-shaped protuberances 32 as well as contact regions 34. This dopant would be n-type if silicon wafer 30 is p-type. As a result as shown in Figure 3 (f), the surface of needle-shaped protuberances 32 as well as contact regions 34 becomes a n-type region 38.

Then as indicated by Figure 3 (g) (top view) and cross-sectional diagram Figure 3 (h), electrode 39 is formed in contact with contact region 34. Electrode 39 my be formed from gold, for example. As explained later, the electrode may be connected to external circuitry using the well-known beam lead structure. Also to prevent alloy formation between the silicon wafer 30 and the gold electrode 39, a barrier metal layer is formed between electrode 39 and silicon wafer 30. It is necessary that electrode 39 should be formed sufficiently shorter than needle-shaped protuberance 32 above the test probe surface so that contact is not made with the test integrated circuit chip during testing.

Next silicon wafer 30 is divided into separate test probe chips. For example during this separation process, the entire needle-shaped protuberance 32

containing surface of silicon wafer 30 is covered by resist, while on the back side of the silicon wafer, the region corresponding to the test probe is covered with resist. The unmasked silicon wafer 30 may be removed by etching so as to open the previously mentioned observation window 14 (Figure 1), so that observation window 14 is formed simultaneous to the division of the silicon wafer into test probe chips.

The test probe of this invention, shown in Figure 3 (i), is formed in the above mentioned manner. Electrodes 39 are formed extending laterally along the entire test probe to form a beam lead structure.

The above mentioned test probe of this invention is fixed to a printed circuit board 1, such as that shown in Figure 7 for the prior art test probe. It is permissible to bond electrode 39 to connector 4. Another mounting technique is to fix the test probe chip into a recess within ceramic substrate 40, as shown in Figure 4, and then to bond electrodes 39 to connections 41. Ceramic substrate 40 is generally stronger than a printed circuit board, easily assuring precise positioning of the test probe as well as a high degree of parallelism between the test probe and the wafer.

In the above mentioned example of the test probe of this invention, the surface of needle-shaped protuberance 32 and the contact region 34 were made to be in electrical contact by the formation of n-type region 38. Therefore if a voltage lower than the range used for test measurements (including the ground) is applied to silicon chip 10, a reverse bias voltage results in the electrical isolation of the respective needle-shaped protuberances 32. It is also possible, for example, to lower the contact resistance of needle-shaped protuberances 32 by covering needle-shaped protuberances 32 with a metallic tungsten or tungsten silicide layer.

It is also possible to electrically mutually isolate needle-shaped protuberances 32 by using an insulation layer. For example, such an electrical insulation structure may be formed by silicon on insulator (SOI) technology. In other words, a SOI 50 is used for test probe fabrication as shown in Figure 5 (a) per the well-known technique. The SOI substrate is formed upon a normal thickness silicon wafer 51 and SiO_2 layer 52. SiO_2 layer 52 is formed upon silicon wafer 51 by thermal oxidation of the wafer surface. Upon this SiO_2 layer 52 is deposited silicon layer 53 by epitaxy at high temperature. The thickness of silicon layer 53 may be later adjusted by chemical mechanical polishing to 12 μm thick, for example. Either the silicon layer may be pre-doped as n-type, or at least the surface layer may be diffusion doped after said polishing step.

Upon this silicon layer 53 surface may be formed needle-shaped protuberances by the same masking procedure as shown in Figure 3. A SiO_2 mask is formed as shown in Figure 5(b). Then needle-shaped protuberances 55 are formed by etching silicon layer 53. Next the remaining silicon layer 53 is

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selectively etched to form separate needle-shaped protuberances 55, as shown in Figure 5 (c). A contact region 56 is provided corresponding to each needle-shaped protuberance 55. A beam lead electrode structure is formed as in the previous working example. Then the silicon wafer is divided into individual chips. The protuberances 55 shown in Figure 5 are electrically isolated from each other by SiO_2 layer 52. Therefore it is not necessary to make provisions for a special reverse bias voltage to be applied to the test probe substrate to isolate the needle-shaped protuberances.

[Results of the Invention] Per this invention a test test probe may be easily made with an array of contacts that correspond to the pads of a high density integrated circuit chip. In comparison to the prior art test probe, these contacts of the test probe of this invention may be positioned with a high degree of accuracy and parallelism with the pads. Also this test probe provided by this invention is more resistant to mechanical collision. Furthermore, damage caused to the pads of the tested integrated circuit chip is decreased, making possible improved production and reliability of high density integrated circuit devices.

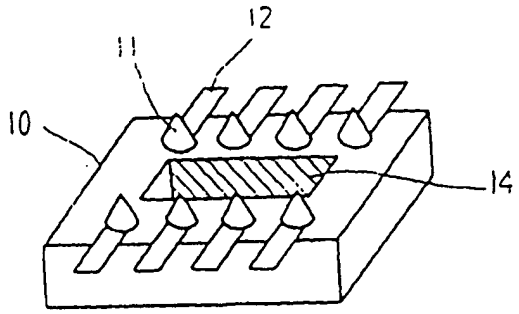

Figure 1. This shows the test probe of this invention.

10. Silicon Chip
11. Probe Contacts
12. Beam Lead Electrodes
14. Visual Observation Window

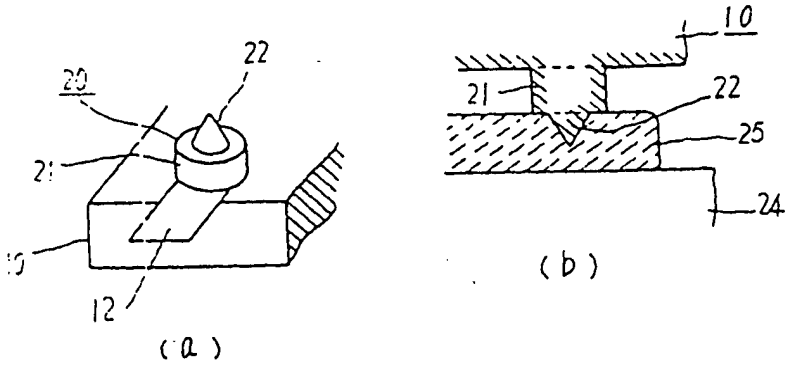

Figure 2. An example of the shape of the probe contact of this invention.

10. Silicon Chip
12. Beam Lead Electrodes
20. Planar Surface
21. Planar Protuberance
22. Probe Contact
24. Integrated Circuit Chip
25. Pad

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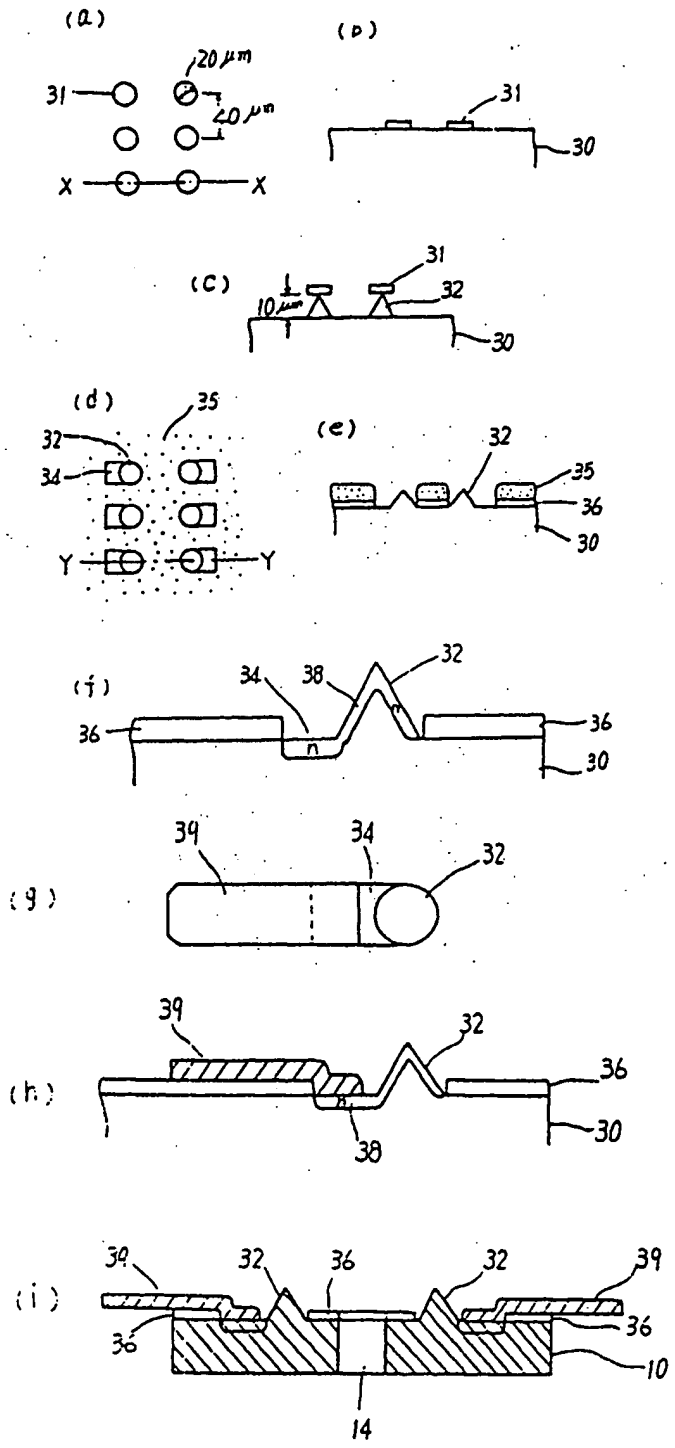

Figure 3. A working example of the construction of the test probe of this invention.

10. Silicon Chip
30. Silicon Wafer
31. SiO_2 Layer
32. Needle-Shaped Protuberance
34. Contact Region
35. Resist
36. SiO_2 Layer
38. n-Type Region
39. Electrode

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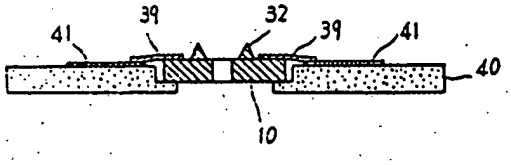

Figure 4. A view of the completed test probe of this invention.

10. Silicon Chip
32. Needle-Shaped Protuberance
39. Electrode
40. Ceramic Substrate
41. Contact

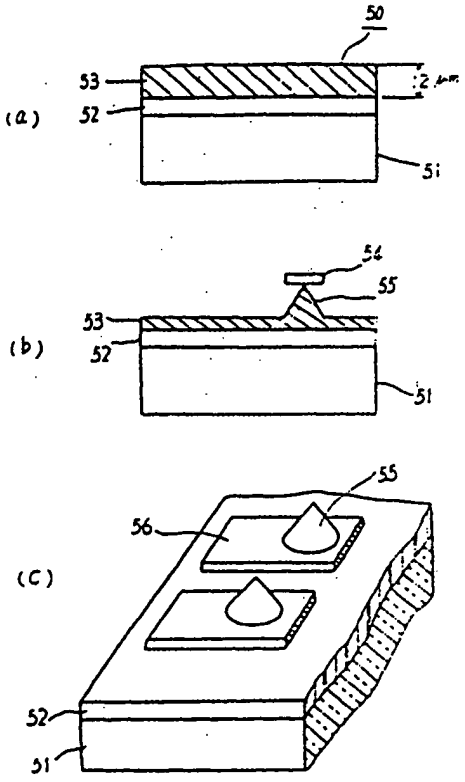

Figure 5. An example of another electrical isolation method for the probe contacts of this invention.

50. Silicon on Insulator
51. Silicon Wafer
52. SiO_2 Layer
53. Silicon Layer
54. Remaining SiO2 Layer
55. Needle-Shaped Protruderance
56. Contact Region

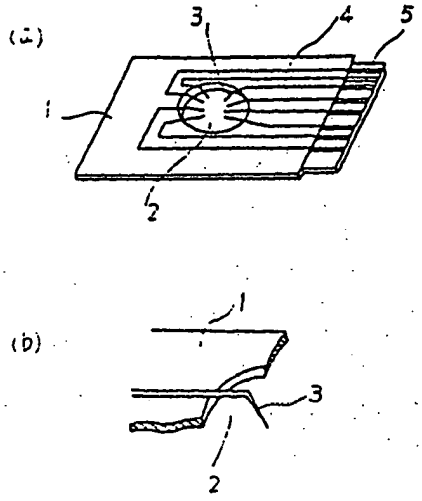

Figure 6. Prior art test probe for testing semiconductor integrated circuits.

1. Printed Circuit Board
2. Aperture
3. Probe Needle
4. Interconnects
5. Board Contacts

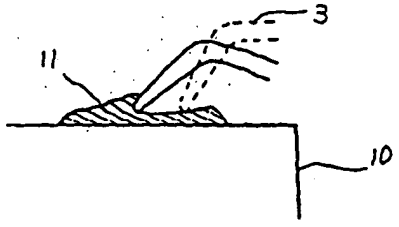

Figure 7. Diagram explaining deficiences of the prior art test probe.

3. Probe Needle
10. Integrated Cricuit Chip
11. Pad